Simulation and Analysis of GaN MIS-HEMT Based Optimized Bootstrap Comparator Applied to DC-DC Buck Converter Feedback Loop

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***Abstract*—This paper presents a feedback circuit topologies based on AlGaN/GaN (Aluminum Gallium Nitride / Gallium Nitride) MIS-HEMT (Metal Insulator Semiconductor High Electron Mobility Transistor) to address the issue of abnormal output ripple in DC-DC buck converters and mitigate voltage overcharge at the operating point. The proposed circuit structure is simulated and calibrated using the ADS (Advanced Design System) platform. Subsequently, the circuit's output characteristics and principles of the optimized bootstrap comparator are analyzed. The results show that the maximum output voltage fluctuation is 0.05 V and the average fluctuation is less than 0.5 %, providing references and suggestions for the feasibility and application potential of the buck converter circuit structure in monolithic integrated GaN power converters.**

***Keywords*—AlGaN/GaN MIS-HEMT, DC-DC Buck Convertor, Bootstrap Comparator, Integrated Circuit**

I. INTRODUCTION

The progress in wide bandgap materials and devices has greatly driven the development of power-integrated circuits [1]. HEMTs (High Electron Mobility Transistors) based on AlGaN/GaN (Aluminum Gallium Nitride / Gallium Nitride) heterostructures exhibit key advantages, including rapid switching capabilities, resilience at high temperatures, and robust breakdown voltage characteristics [2-8]. These traits render them invaluable as primary switches in power converters.

For DC-DC converter, maintaining output voltage stability is a critical challenge due to fluctuations in input line voltage and non-linear changes in load resistance with temperature [9]. To tackle this issue, a feedback strategy was implemented to monitor and adjust the driver stage input signal [10]. Sun et al. developed a 29 V input / 10 V output DC-DC buck converter integrated feedback solution based on GaN power IC platform to ensure relatively stable voltage maintenance [9]. However, this design still exhibits a consistent output ripple (approximately 0.4V), and the presence of output ripple can significantly impact signal quality in scenarios involving low output voltage and low output/input ratio.

This work proposes an optimized bootstrap comparator based on AlGaN/GaN MIS-HEMT, aiming to optimize performance through a modulated signal feedback loop, followed by a detailed parameter analysis. These circuit topologies are simulated using the ADS (Advanced Design System) platform to evaluate performance compared to prior arts, focusing on the suppressive effect of the optimized dual-stage comparator's feedback loop on the output ripple of the buck converter.

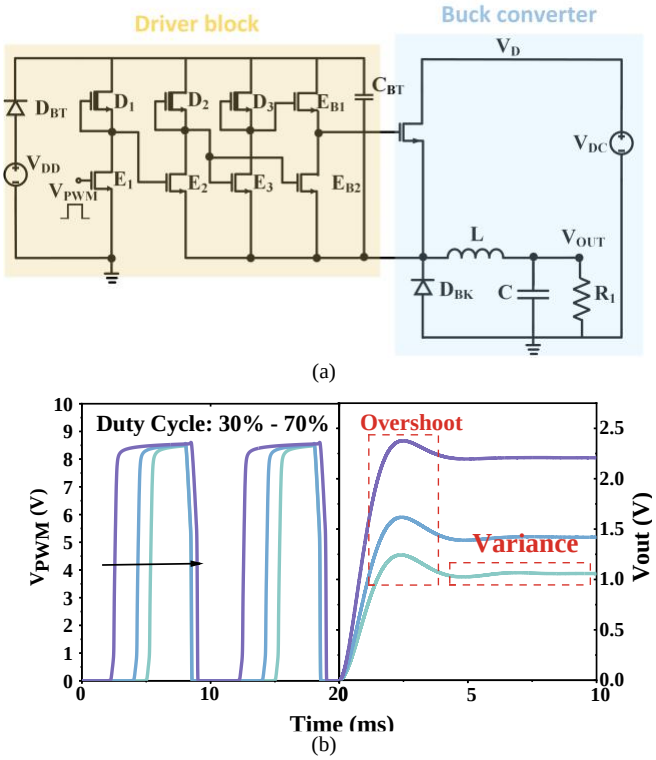


Fig. 1 The conventional topology of buck converter. (b) Output characteristics of different duty cycles of PWM input.

II. SIMULATION STRUCTURES AND DISSCUSTION

A. Conventional buck converter with feedback loop

The MIS-HEMT D/E-mode device parameters in the ADS platform are established following the methodology and results presented in the GaN-based ASM (Advanced spice model)-HEMT research by Lu et al. [11]. The circuit topology of a DC-DC buck converter with a feedback loop is shown in Fig. 2. A bootstrap comparator performs logical judgments by comparing the V_{SAMPLE}, sampled by the R2/R3

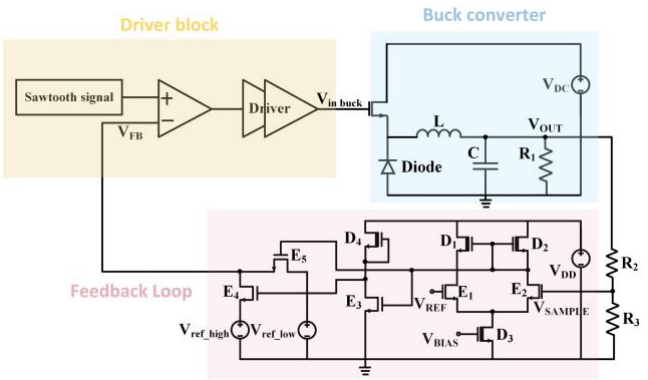
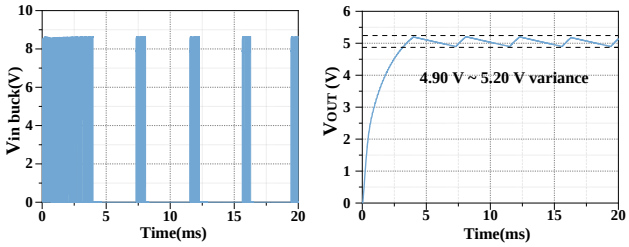


Fig. 2 Schematic diagram of feedback loop circuit designed for DC-DC buck converter.



(a) (b)

Fig. 3 Input (a) and Output (b) signal of DC-DC buck converter with feedback loop modulation.

resistive divider, with the reference voltage V_{REF}. If V_{SAMPLE} is lower than V_{REF}, the comparator outputs a high-level signal, turning on E_3 and E_5. This causes the reference end of the PWM generator's comparator in the driver stage to connect to a low voltage signal, thereby modulating the increase of the PWM signal's duty cycle, which raises the buck output voltage V_{DC}. Conversely, if the comparator outputs a low-level signal, E_3 and E_5 turn off, and a high-level signal is connected to the reference end of the PWM generator's comparator in the Driver stage, modulating a decrease in the output voltage V_{DC}.

Considering the verification of the feasibility of this feedback circuit, the operating condition of the circuit is simulated and analyzed as follows. The $V_{in\ buck}$ signal demonstrates in Fig. 3(a) is generated based on the V_{FB} and the sawtooth input signal. When the V_{REF} is set to 4.8 V, the output signal from the feedback loop (V_{FB}) is connected to the source signal V_{ref_low} (2 V) if the output of the bulk converter is lower than 4.8 V. Therefore, the $V_{in\ buck}$ generates a specified duty cycle PWM signal until the V_{OUT} exceeds 4.8V. After the V_{OUT} exceeding 4.8 V, the feedback loop is switched output the source signal V_{ref_high} (10 V) which will cause an output logic low to $V_{in\ buck}$ for a specific time until the V_{OUT} decreased to potential lower than 4.8V. As shown in Fig. 3(b), the V_{OUT} signal can be maintained around 5 V by adjusting the $V_{in\ buck}$ input signals with different duty cycles after the introduction of the feedback different duty cycles after the introduction of the feedback loop, which oscillates in the range of 4.90-5.20 V, with an average

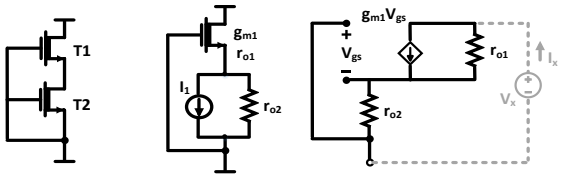


Fig. 4 The small signal analysis of the optimized load.

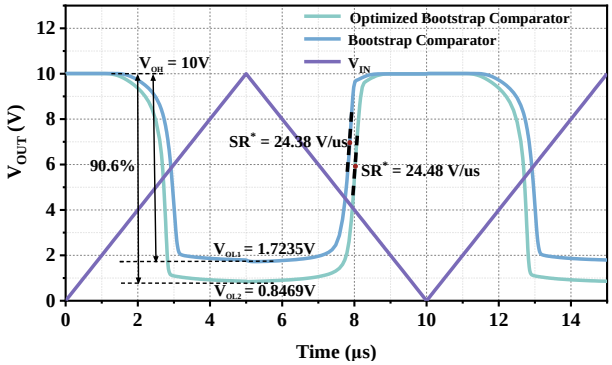


Fig. 5 Output characteristics of an optimized bootstrap comparator and a bootstrap comparator under transient simulation.
*SR (Slew Rate) is defined as the maximum rate of change of output voltage per unit time ($\Delta V_{OUT}/\Delta t$).

oscillation of 0.15 V, and a fluctuation rate of 3%. Although this feedback loop topology can effectively solve the voltage overshoot phenomenon at the operating point, the suppression of output fluctuation is limited.

B. Feedback loop by optimized bootstrap comparator

In the case of the bootstrap comparator in the feedback loop, voltage fluctuations around 0.15 V reluctantly ensure a stable output voltage signal. However, for active loads, this structure results in a higher output resistance, which results in a larger gain and still too large a difference in the output stage. In order to find a better solution, a small-signal analysis of the optimised load is first performed:

Apply Thevenin's theorem:

$$V_{gs} = -i_x r_{o2}$$

$$i_x = g_{m1}V_{gs} + \frac{V_x - (-V_{gs})}{r_{o1}}$$

Then, the output resistance becomes:

$$r_{o,eq} = \frac{v_x}{i_x} = g_{m1}r_{o1}r_{o2} + r_{o1} + r_{o2} \approx g_{m1}r_{o1}r_{o2}$$

The output resistance has improved by factor $g_{m1}r_{o1}$, which means the gain of the comparator is larger, resulting in a faster transition time. In the design process, the size of the upper D-mode load is typically five times larger than the subsequent D-mode stage. This is due to two main reasons: (I) The larger width increases g_{m1}, leading to a faster transition time. (II) The lower transistor is fabricated with a short channel effect, and a larger transistor results in lower conducting resistance, ensuring the transistor operates in the saturation region.

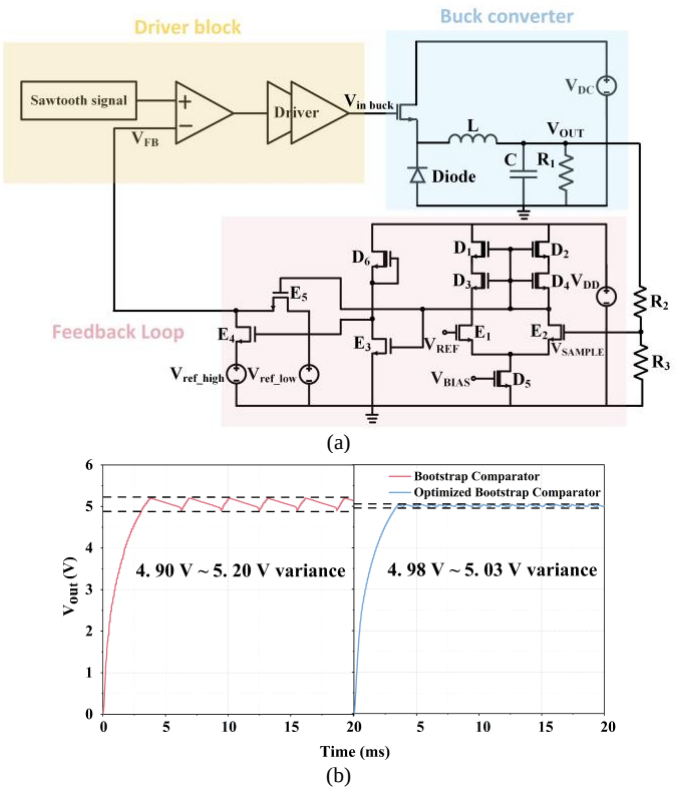


Fig. 6 (a) The circuit diagram of a buck converter with feedback loop improved by optimized bootstrap comparator. (b) Comparison of output characteristics of two mentioned feedback loop designs.

To further validate the theoretical assumption and achieve a more stable V_{OUT}, a comparison of the transient output characteristics of the two comparator topologies is shown in Fig. 5. The output swing of the optimized bootstrap comparator is nearly 10% higher than the other, and its slew rate is improved by 0.1 V/μs due to larger gain from load. Furthermore, the above optimization structure is applied to the feedback loop, and the resulting circuit diagram is shown in Fig. 6(a). The feedback loop utilizing the optimized bootstrap comparator is able to produce a more stable 5 V output signal for V_{OUT}, and its fluctuation is reduced from 0.3 V to 0.05 V, with lower fluctuation rate of 0.05%. The main parameters of the MIS-HEMT used for simulation are listed in Table 1.

IV. CONCLUSION

In conclusion, this study delves into two feedback loops for DC-DC buck converters based on AlGaN/GaN MIS-HEMT devices. Simulations were conducted to analyze the circuit performance concerning the abnormal output ripples and alleviate overvoltage of the working point. Additionally, the optimized bootstrapped comparator is confirmed by simulation results to have an enhancing effect on the regulation of the feedback circuit. And the calculations and simulation results offer guidance for designing a feedback loop for a DC- DC buck converter with a more stable output signal. Consequently, this work contributes to the application potential of the feedback loop for the DC-DC buck converter designs, offering guidance for their integration into diverse circuit applications. In the next study phase, further aspects will be considered to conduct a more comprehensive evaluation of the circuit design.

TABLE 1. KEY PARAMETERS FOR THE CIRCUIT SIMULATION

Category	Parameters	Values (μm)
Comparator	D-mode MIS-HEMTs **$D_{1,2,3,4}$**	$L_{GS}/L_G/L_{GD}$ = 15/3/5 $W_{1,2}$ = 200 W_3 = 15 W_4 = 20
	E-mode MIS-HEMTs **E_1 E_2**	$L_{GS}/L_G/L_{GD}$ = 5/3/5 $W_{2,3}$ = 200
Inverter	D-mode MIS-HEMT **D_6**	$L_{GS}/L_G/L_{GD}$ = 15/3/5 W_6 = 10
	E-mode MIS-HEMT **E_4**	$L_{GS}/L_G/L_{GD}$ = 5/3/5 W_4 = 100
Others	E-mode MIS-HEMTs **$E_{5,6}$**	$L_{GS}/L_G/L_{GD}$ = 5/3/5 $W_{5,6}$ = 100

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